ABSTRACT OF THE DISCLOSURE

A processor is disclosed that can map a request from a central processing unit that uses memory-mapped input-output space to a second processing domain, such as a multithreaded processing domain. A request addressed to the input-output space of the central processing unit is converted to a corresponding command that simulates an operation between components in the multithreaded processing domain. The command is executed in the multithreaded processing domain. Information is accessed according to the request in response to executing the command.

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